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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,093	09/26/2003	Tazrien Kamal	AF01139.D1	7095

22898 7590 08/10/2004

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,093	KAMAL ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Preliminary Amendment

In Preliminary Amendment, applicant cancels claims 11-20. Claims 1-10 are remained for examination.

Claim Objection

Claims 1, 10 are objected as following:

In claim 1, "a dielectric layer over the wordline" should be amended to --- an interlayer dielectric layer over the wordline---,

and "the dielectric layer, and a combination thereof." at the end of claim 1 should be amended to --- the interlayer dielectric layer, and a combination thereof. ---

In claim 10, "the method of manufacturing an integrated ciruict as claimed in claim 1" should be amended to --- the method of manufacturing an integrated ciruict as claimed in claim 6----

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 USC 102 (e) as being anticipated by Ramkumar et al., U.S. Patent No. 6,6777,213.

Regarding claim 1, Ramkumar et al. discloses the method of forming an integrated circuit (IC) similar to what recited in claim 1. See Figs. 1-8 and Cols. 1-12. The method comprising:

. forming a charge-trapping dielectric layer 20 over a substrate 12 (fig. 1);

. forming first and second bitlines in the substrate (26, Fig. 1);

. forming a wordline 22 (Figs. 2-3) over the charge-trapping dielectric layer (polysilicon 22, lines 1-3, Col. 6);

. forming an interlayer dielectric layer 36 (fig. 4) over the wordline wherin for a structure selected from at least one of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof, the structure contains deuterium diffused from another structure selected from at least one of the charge-

trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof (lines 10-25, Fig. 3, deuterium diffused from layer 22 to layer 20).

Regarding claim 6, Ramkumar et al. discloses the method of forming an integrated circuit (IC) similar to what recited in claim 6. See Figs. 1-8 and Cols. 1-12. The method comprising:

. forming a first dielectric layer 14 in a substrate 12 (fig. 1);

. forming a charge-trapping dielectric layer 16 over the first dielectric layer (fig. 1);

. forming a second dielectric layer 18 over the charge-trapping layer (fig. 1);

. forming first and second bitlines in the substrate (26, Fig. 1);

. forming a wordline 22 (Figs. 2-3) over the charge-trapping dielectric layer (polysilicon 22, lines 1-3, Col. 6);

. forming a spacer 24 around the wordline (fig. 1)

. forming an interlayer dielectric layer 36 (fig. 4) over the wordline wherein for a structure selected from at least one of the first and second dielectric layers, the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, the spacer, and a combination thereof, the structure contains deuterium diffused from another structure selected from at least one of the first and second dielectric layers, the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, the spacer, and a combination thereof (lines 10-25, Fig. 3, deuterium diffused from layer 22 to layer 20).

Regarding claims 2-3 and 7-8, Ramkumar et al. discloses the IC as in claims 1 and 6 above, and further discloses forming deuterated materials for a structure selected from at least one of the first and second dielectric layers, the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, the spacer, and a combination thereof (lines 10-25, Fig. 3, deuterium diffused from layer 22 to layer 20; fig. 7, Cols. 8-9).

Regarding claims 4 and 9, Kamkumar et al. discloses the method above and further discloses wherein the first and second dielectric layers, the charge-trapping layer, the wordline, the spacer, the interlayer dielectric layer deposits material selected from at least one of a deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a polysilicon, a glass, and a combination thereof (silicon oxide layers 14 and 18, silicon nitride layer 16, polysilicon layer 22 etc...Figs. 1-8).

Regarding claims 5 and 10, Kamkumar et al. discloses the method above and further discloses wherein the forming of the first and second dielectric layers, the charge-trapping layer, the wordline, the spacer, the interlayer dielectric layer using the methods selected from a group consisting of CVD, annealing in deuterium gas, rapid thermal oxidation (lines 10-21, Col. 5; lines 46-65, Col. 6).

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800